WHAT IS CLAIMED IS:

1. A signal transmission circuit, including:

a plurality of signal paths which respectively transmit signals outputted from a plurality of different circuit elements; and

an output path formed by connecting the plurality of signal paths,

wherein each of the plurality of signal paths includes a buffer element and a switching element which receives an output from the buffer element, the output path is formed by connecting output lines of the switching elements, there is disposed a buffer element in the output path, and wherein any of the switching elements in the plurality of signal paths is turned on according to an operational mode, and then a target signal is selected and outputted to the output path.

2. A signal transmission circuit according to Claim 1, wherein the buffer elements are disposed in a dispersed manner so that the target signal might obtain a desired output characteristic by passing through both the buffer elements provided in the plurality of signal paths and the buffer element provided in the output path.

3. A signal transmission circuit according to Claim 1,

wherein each of the different circuit elements is one corresponding to a final-stage circuit element in a block which sequentially drives a plurality of pixel circuits, when the pixel circuits are driven in a forward or reverse direction, and the operational mode is switched corresponding to the forward or reverse direction of driving the pixel circuits.

4. A signal transmission circuit according to Claim 3, further including a signal path up to a connector pin from the final-stage circuit element, wherein the buffer element disposed in the vicinity of the circuit element and the buffer element disposed in the vicinity of the connector pin are provided in the signal path, and wherein the plurality of buffer elements necessary for a signal to be transmitted to finally have a desired output characteristic are disposed in a dispersed manner.

5. A signal transmission circuit according to Claim 2, wherein each of the different circuit elements is one corresponding to a final-stage circuit element in a block which sequentially drives a plurality of pixel circuits, when the pixel circuits are driven in a forward or reverse direction, and the operational mode is switched corresponding to the forward or reverse direction of driving the pixel circuits.

6. A display apparatus, including:

a plurality of pixel circuits;

a circuit block which sequentially drives the plurality of pixel circuits;

a plurality of signal paths that transmit signals outputted from circuit elements in the circuit block which respectively correspond to a final stage of the circuit block, when the pixel circuits are driven in a forward or reverse direction; and

an output path formed by connecting the plurality of signal paths,

wherein each of the plurality of signal paths includes a buffer element and a switching element which receives an output from the buffer element, the output path is formed by connecting output lines of the switching elements, there is disposed a buffer element in the output path, and wherein any of the switching elements in the plurality of signal paths is turned on according to a drive direction in the circuit block, and then a target signal is selected and outputted to the output path.

7. A display apparatus according to Claim 6, wherein the circuit block is a circuit which drives a data signal line for writing data to the plurality of pixel circuits.

8. A display apparatus according to Claim 7, wherein the circuit block is a shift register, and the plurality of signal paths transmit signals outputted from a final-stage of the shift register.

9. A display apparatus according to Claim 6, wherein the circuit block is a circuit which drives a scanning line for writing data to the plurality of pixel circuits.

10. A display apparatus according to Claim 9, wherein the circuit block is a shift register, and the plurality of signal paths transmit signals outputted from a final-stage of the shift register.

11. A signal transmission circuit according to Claim 6, wherein the buffer elements might be disposed in a dispersed manner so that the target signal might obtain a desired output characteristic by passing through both the buffer elements provided in the plurality of signal paths and the buffer element provided in the output path.

12. A display apparatus according to Claim 6, wherein the buffer elements provided in the plurality of signal paths are adjusted so as to have a substantially uniform characteristic therebetween.

13. A display apparatus according to Claim 6, further including a signal path up to a connector pin from the final-stage circuit in the circuit block, wherein the buffer element disposed in the vicinity of the circuit element and the buffer element disposed in the vicinity of the connector pin are provided in the signal path, and wherein the plurality of buffer elements necessary for a signal to be transmitted to finally have a desired output characteristic are disposed in a dispersed manner.

14. A signal transmission circuit, including a signal path up to a connector pin from a circuit element disposed at a final stage of a circuit block which sequentially drives a plurality of pixel circuits, wherein a buffer element disposed in the vicinity of the circuit element and a buffer element disposed in the vicinity of the connector pin are provided in the signal path, and wherein the plurality of buffer elements necessary for a signal to be transmitted to finally have a desired output characteristic are disposed in a dispersed manner.